16. A semiconductor device comprising:

a substrate; and

a gate structure on the substrate, the gate structure comprising a layer of semiconductor material overlying the substrate, a layer comprised of a metal overlying the layer of semiconductor material, a layer comprised of polycrystalline silicon overlying the layer comprised of a metal, a layer of silicide overlying the layer comprised of polycrystalline silicon and a cap layer overlying the layer of silicide.

17. The semiconductor device of claim **16**, where the cap layer comprises a nitride.

18. The semiconductor device of claim **16**, further comprising: an interlevel dielectric that at least partially overlies the gate structure; and a borderless contact comprised of a metal.

19. The semiconductor device of claim **18**, where the interlevel dielectric comprises an oxide with a nitride liner.

20. The semiconductor device of claim **18**, where the semiconductor device comprises a metal oxide semiconductor field effect transistor.

21. A semiconductor device comprising:

a substrate;

a gate structure on the substrate, the gate structure comprising a metal gate core that is adjacent to a layer of dielectric material on at least two surfaces of the metal gate core; and

a cap layer overlying the layer of dielectric material and the metal gate core.

22. The semiconductor device of claim **21**, where a top surface of the metal gate core is not covered by the layer of dielectric material.

23. The semiconductor device of claim **21**, where the at least two surfaces comprise at least one sidewall surface and a bottom surface.

24. The semiconductor device of claim **21**, where the at least two surfaces do not comprise a top surface of the metal gate core.

25. The semiconductor device of claim **21**, further comprising: an interlevel dielectric that at least partially overlies the gate structure; and a borderless contact comprised of a metal.

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